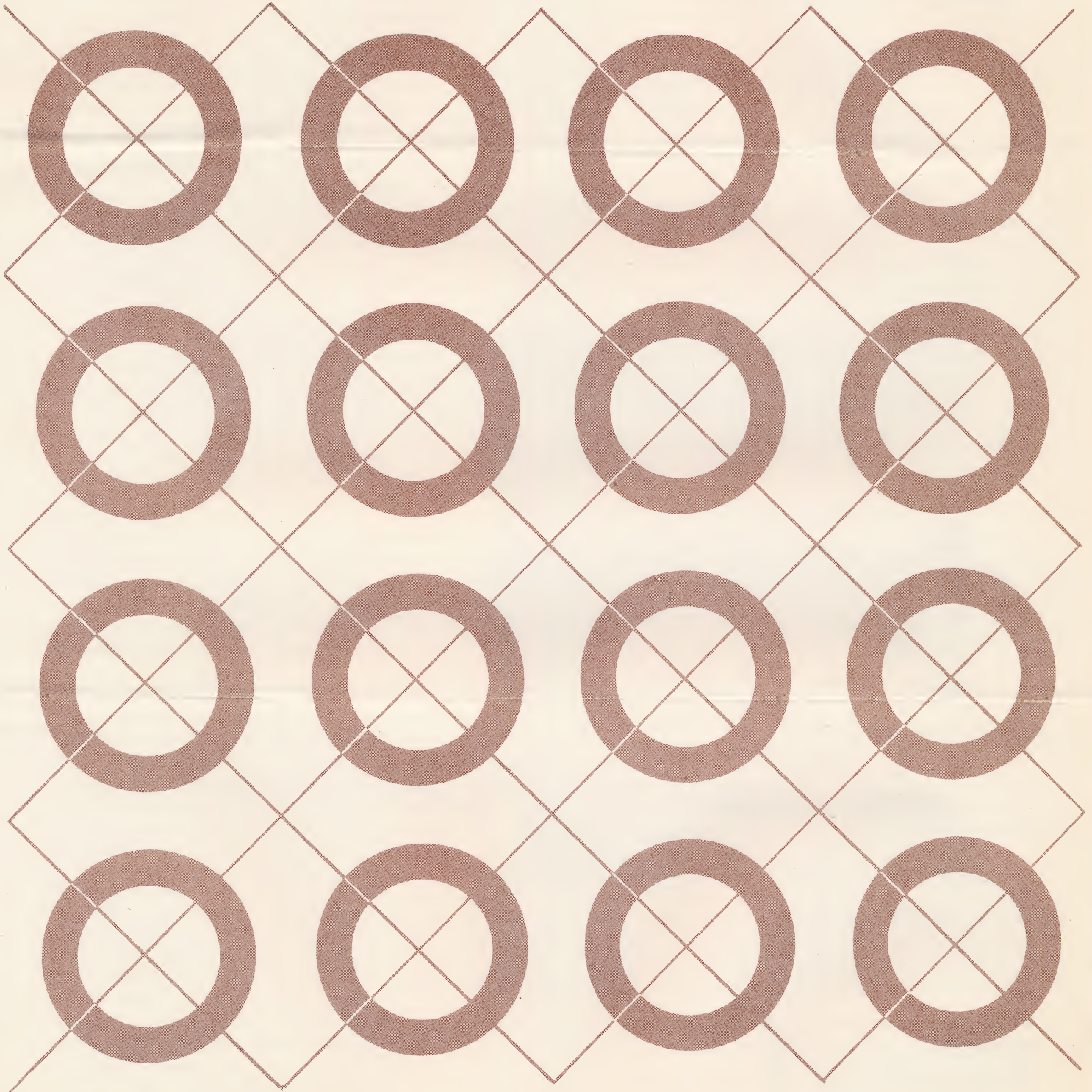# ministore III A

a new low cost core memory

A Value-Engineered Memory

David M. Biberman, *President, Rese Engineering, Inc., Philadelphia, Pa.*

(From an article in Computer Design)

Charging and Discharging Current of Capacitors Switches Memory Cores

The Ministore memory system opens like a book, however, it is not a read-only memory.
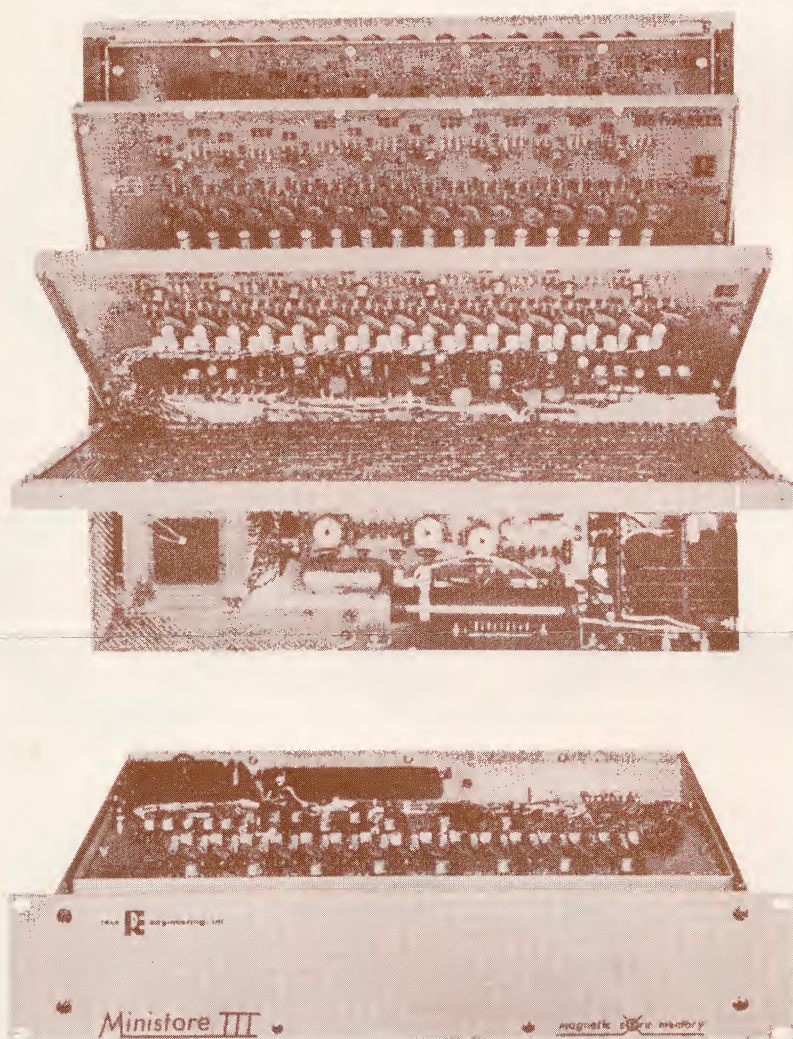
Most of the new development work on memory design is directed toward increasing speed and capacity while reducing physical size. And great strides have been made in achieving these objectives. However, for many applications — memory buffer for input/output equipment, format control, data communications, special purpose data handling systems, quick look-up tables, etc. — higher speeds are not essential and cost becomes the all-important criterion.

With the above applications in mind and with low cost the prime objective, Rese Engineering, Inc., developed a "Value Engineered" memory system. The most recent unit is called the Ministore III-A.

A novel circuit and packaging technique are the key features that contribute to the lower cost of the Ministore memory without sacrificing quality and reliability. In the Ministore, the charging and discharging current of capacitors is used to switch the magnetic state of memory cores. This circuit arrangement requires fewer active components, decreasing cost and also increasing reliability.

By choosing an optimum number of addresses and word lengths, a package design has been achieved which uses a single, universal circuit board which accommodates the complete range of Ministore capabilities. This simplifies manufacturing and reduces the cost of production. A mechanical package, opening like a book, has eliminated all internal mechanical connectors, increasing long term reliability and again decreasing cost.

Maintenance is greatly simplified since there is just one type of board with each component clearly designated and easily accessible. A large number of specified check points further facilitates easy maintenance.
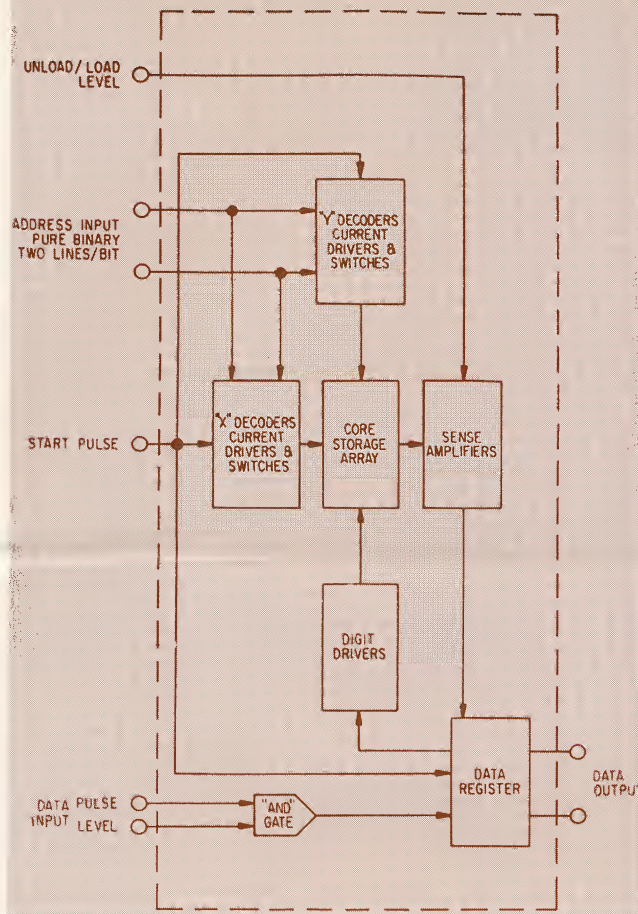
Block diagram of the Ministore memory

MINISTORE III A

A complete, low cost, random access memory for use in:

- **INPUT/OUTPUT BUFFERING**

- **TAPE STORAGE BUFFERING**

- **DATA COMMUNICATIONS**

- **FORMAT CONTROL**

- **DATA DISPLAY SYSTEMS**

- **SPECIAL PURPOSE DATA SYSTEMS**

- **SMALL COMPUTER WORKING MEMORY**

Here is a complete random access, ferrite core memory with an outstanding specification — price. Compact, modular and miniaturized, Ministore is completely Value Engineered from its unique circuit design to its superior packaging technique. And its price tag is less than half that of other memories. Available in a number of word lengths and addresses. Ministore III A opens up a new area of application for random access storage techniques.

For memory applications involving faster speeds, larger capacities, and other operating modes, ask for information describing the new Rese 6500 Series.

For complete details or a demonstration, contact:

rese **RE** engineering, inc.

A & Courtland Sts.,

Philadelphia, Penna. 19120

215-GL 5-9000

rese

Addressing of the memory is straight binary, two lines per bit, providing a unique location for all addresses from the first to the maximum address. The memory operates on either a Read/Regenerate (Unload) or a Clear/Write (Load) cycle. It operates in the same manner in both the Unload cycle and the Load cycle, the only difference being the application of a Load or Unload level to signal which cycle is desired. In the Load cycle, data must be applied to the data register input.

In the Read/Regenerate cycle, the Load/Unload level must be at 0 volts. Upon receipt of the start pulse, the data register is cleared and the input address lines interrogate the core stack. The information contained in the addressed cores is read-out and stored in the data register. This information is available within 4 usecs (access time). At the trailing edge of the start pulse, the write pulse "restores" the information contained in the data register into the cores from which it was taken.

In the Clear/Write cycle, the Load/Unload level must be at -6 volts. Upon receipt of the start pulse, the data register is cleared. The Load level inhibits the sense amplifier gate and prevents the data from being read-out from the addressed cores to the data register.

Data is applied to the data register inputs through a resistor/capacitor gate, affording two options for presenting the data — as a pulse or as a level which is clocked-in.

During the write portion of the cycle, the new data in the data register is written into the memory. The input word must be presented in parallel. The data register holds this word until the start of the next cycle, at which time the start pulse clears the data register.

The Ministore III-A is a random access core memory with storage capacities ranging from 64 to 2048 words. Word lengths range from 2 to 24 bits. Access time is less than 4 microseconds and the full cycle time is 10 microseconds. The smallest memory, 64 x 2, is priced at $1100; a 1024 x 8 is priced at $3080.

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MINISTORE III A

SPECIFICATIONS

FUNCTIONAL

Capacity	64 to 2048 words
Word Size	2 to 24 bits per word
Access Time	4 μsec
Full Cycle Time	10 μsec
Mode of Access	random-parallel
Commands	(1) READ/REGENERATE (UNLOAD)
	(2) CLEAR/WRITE (LOAD)
Address	straight binary—parallel—two lines per bit
Input Data	MODE: Parallel
	FORM: Information can be presented as (a) a Level which is clocked in, or (b) in the form of a positive going pulse
Output	MODE: Parallel. Two lines per bit
	FORM: DC Level

POWER REQUIREMENTS

Negative Voltage:
  −15 to −30 volts
  4.0 amps maximum
Positive Voltage:
  +12 to +30 volts
  0.5 amps maximum
These voltages are regulated to ±12 volts ±1% in the MINISTORE III

MECHANICAL

Size	19" W. x 3½" H. x 16½" D.
Finish	Satin Anodized Aluminum
Connections	All external connections via (2) Amphenol 50 pin micro ribbon connectors
Mounting	Standard relay rack mounted
Cooling	Convection cooled
Weight	20 lbs.

ENVIRONMENTAL

Operating Temp.	0° to +50°C
Storage Temp.	−20° to +60°C
Relative Humidity	0% to 90%

INPUT

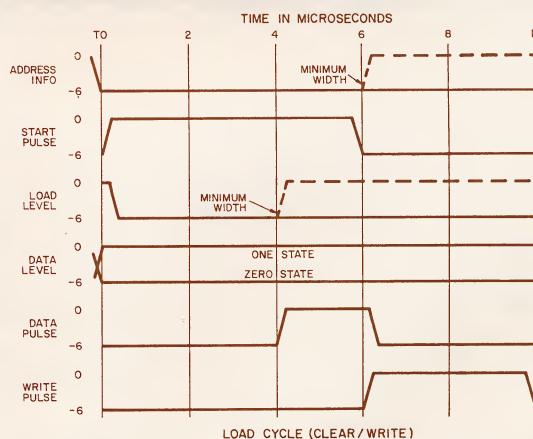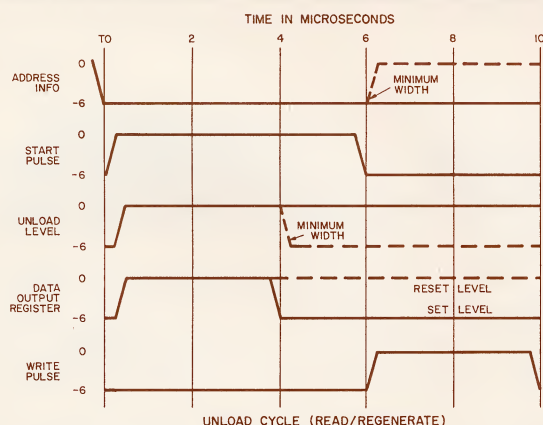|	
Start Pulse	Positive-going pulse (−6 to 0 volts) Pulse width: minimum 6 μsecs Rise and Fall Time: less than 1 μsec Loading: 15 ma, 1000 pf
Write Pulse (Internally Generated)	Positive-going pulse (−6 to 0 volts). Must follow the trailing edge of Start pulse to ±1 μsec Pulse width: 4 μsecs ±1 μsec Rise and Fall Time: less than 1 μsec Loading: 15 ma, 1000 pf
Load/Unload Level	UNLOAD: 0 volts LOAD: −6 volts A voltage which must be quiescent within .5 μsec after start pulse and have a minimum width of 4 μsec Rise and Fall Time: not critical Loading: 15 ma, 1000 pf
Address Information	Pure binary, two lines per bit, must be quiescent during entire period of start pulse TRUE: −6 volts FALSE: 0 volts Rise and Fall Time: not critical Loading: 15 ma maximum, 1000 pf
Data Information	Input through R-C gate 1. Level Input: 0 volts = ONE; −6 volts = ZERO Level must be applied to resistor input at least 2 μsecs before positive-going clock pulse is applied to the capacitor input. The clock pulse width must be greater than 1 μsec, and Rise and Fall Time less than .5 μsec Loading: 2 ma, 680 pf 2. Pulse Input: Resistor grounded and *positive-going* pulse applied to capacitor represents a ONE Data Pulse: between 1 and 4 μsec duration; .5 μsec rise and fall time

OUTPUT

Both collectors are available as outputs from the data register
Loading: 10 ma, DC can be delivered from ground; 3 ma, DC can be delivered from −12 volts
Maximum capacitor load: 1000 pf

UNLOAD CYCLE (READ/REGENERATE)

LOAD CYCLE (CLEAR/WRITE)

PRICE LIST

Effective

September 1, 1965

MINISTORE IIIA

Random Access Magnetic Core Memories

10 microsecond, full cycle

-------------- NUMBER OF WORDS (ADDRESSES) --------------

NUMBER OF BITS PER WORD (WORD LENGTH)	64	128	256	512	1024	2048
2	$1,100	$1,240	$1,400	$1,650	$1,990	$2,610
4	1,290	1,430	1,670	1,970	2,360	3,020
6	1,560	1,730	1,940	2,290	2,720	3,440
8	1,840	2,020	2,220	2,610	3,080	3,840
10	1,970	2,170	2,490	2,830	3,450	
12	2,160	2,350	2,760	3,250	3,810	
14	2,350	2,590	3,030	3,570	4,170	
16	2,540	2,800	3,300	3,890	4,540	
18	2,780	3,020	3,580			
20	2,970	3,290	3,840			
22	3,170	3,510	4,120			
24	3,360	3,720	4,400			

NOTE: For other capacities, speeds, and operating modes, check into the Rese 6500 Series modular memories.

The above prices are f.o.b. factory, Philadelphia, Pennsylvania, packed for domestic shipment, and are subject to change without notice. Prices in quantities or custom requirements furnished upon request.

PLEASE FURNISH POWER SUPPLY VOLTAGES AVAILABLE WHEN ORDERING (see catalog sheet).